

REMARKS/ARGUMENTS

This amendment is in response to a Final Office Action mailed October 28, 2004. No claim amendments have been made.

On January 25, 2005, a telephone conference was conducted between the undersigned attorney and the Examiner. The discussion was directed to claim construction for various terms and the absence of limitations set forth in the independent claims. While no agreement was reached, Applicant has agreed to refrain from filing of a Notice of Appeal in order to allow the Examiner to consider whether the finality of the rejection should be withdrawn. The undersigned attorney wishes to formally thank the Examiner for his time and attention to this matter.

With respect to the IDS submission filed on September 17, 2004, Applicant has fully complied with and has gone beyond his duty of disclosure under 37 C.F.R. §1.56. In the telephone conference, the Examiner respectfully requested that the undersigned attorney provide a list of references that, upon his brief review, may be relevant to examination. The undersigned attorney has conducted a review and provides such a listing for the Examiner as noted below. For the record, this list should not be construed by the Examiner as a complete listing of all cited references material to the examination. In addition, the list should not be construed as an admission that any of the cited references are even material to the examination. The cited references were merely obtained from a search of art in the same technical area. In fact, some of the cited references do not constitute prior art references, but were supplied merely to advise the Examiner of co-pending applications. The undersigned attorney respectfully requests the Examiner to thoroughly review the references and make a determination based on his review. The ordering of the list is chronological, based on earliest publication or issue date.

Relevant Prior Art References: 2002/0087765; 2002/0087766; 2002/0087804; 2003/0065843; 2003/0070016; 2003/0131201; 2003/0131202; USP 6,598,123; USP 6,615,319; USP 6,622,215; 2003/0177317; and USP 6,704,845.

Relevant References (Not Prior Art): 2002/0129206; 2003/0126376; 2003/0135696; 2003/0163649; 2003/0177320; 2003/0204679; and 2004/0022094.

Rejection Under 35 U.S.C. § 102

Claims 1-7 and 9-30 were rejected under 35 U.S.C. §102(e) as being anticipated by Mackenthun (U.S. Patent No. 6,374,332). Applicant respectfully traverses the rejection and contends a *prima facie* case of anticipation has not been established.

As the Examiner is aware, to anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

The first ground for traversing the rejection is based on the interpretation of a processor, namely the processor (350A) of Mackenthun, as an "input-output device." The specification is clear that the input-output device may be a bridge for example. *See Paragraph 7 of subject application*. According to an on-line encyclopedia (Wepopedia; Exhibit A), an input-output device is "any program, operation or device that transfers data to or from a computer and to or from a peripheral device." A processor does not constitute an input-output device as commonly used in the technology field. Hence, based on this ground alone, Applicant respectfully requests the Examiner to withdraw the finality of the outstanding Office Action and reconsider the allowability of the claims.

With respect to the second ground for traversing the rejection, it is alleged that the "address logic circuitry" corresponds to circuitry for comparing read request addresses to pending write addresses as discussed at column 15, lines 10-15 of Mackenthun. *See Page 3, paragraph 4 of the Final Office Action*. Upon review, column 15, lines 10-15 of Mackenthun describes the operations of the Write Buffer Logic 434, Write Request 2 Logic 438 and Write Request 1 Logic 454, where conflicts are signaled to Processing Logic 402 on lines 462 and 468. It is further alleged that the ownership pre-fetch circuitry is the bus snooping logic 432. *See Page 3, paragraph 4 of the Final Office Action*.

Applicant respectfully submits that a *prima facie* case of anticipation has not been established because Mackenthun does not teach the coupling of the ownership pre-fetch circuitry to the address logic circuitry. More specifically, Applicant respectfully submits that anticipation cannot be established because the bus snooping logic 432, considered to be equivalent to the ownership pre-fetch circuitry (irregardless whether or not such interpretation is agreed upon by the Applicant), is not coupled with the address logic circuitry as set forth in claims 1 and 24.

Furthermore, in addition to the arguments set forth above, Mackenthun does not provide any teachings that the bus snooping logic 432 initiates a request for ownership of a first memory content associated with a first address for the first transaction (READ transaction per Final Office Action) unless the first address is substantially equivalent to the second address (address of WRITE transaction per Final Office Action).

Hence, based on the second ground for traverse, Applicant respectfully requests the Examiner to withdraw the finality of the outstanding Office Action and reconsider the allowability of the claims.

With respect to a third ground for traversing the rejection, it is alleged that the “transaction bypass circuitry” of claim 5 corresponds to circuitry for accessing the third level cache (TLC) 310 and/or crossbar module (TCM) 220 for accessing main storage 110. Applicant respectfully disagrees with this analysis. Claim 5 includes the limitation that the transaction bypass circuitry is “coupled with said input-output interface.” Since the input-output interface is considered in the Final Office Action to be interface 370A of Mackenthun, the transaction bypass circuitry would have to be considered a component of the second level cache (360A) of Mackenthun, namely either controller 426 or Data RAM logic 420. None of these components, however, operate as the transaction bypass circuitry as claimed.

Based on the third ground for traverse, Applicant respectfully requests the Examiner to withdraw the finality of the outstanding Office Action and reconsider the allowability of the claims.

Conclusion

In view of the foregoing, Applicant contends that a prima facie case of anticipation has not been established and respectfully requests the Examiner to allow all of the pending claims. Allowance of these claims at Examiner's earliest convenience is respectfully solicited.

In order to further facilitate prosecution of the subject application, Applicants respectfully request the Examiner to contact the undersigned attorney at the phone number listed below to coordinate an Examiner's interview to discuss the allowability of the pending claims, if such discussion is warranted. The undersigned attorney can be reached at the telephone number listed below.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: January 28, 2005

By


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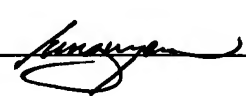
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Short for *input/output* (pronounced "eye-oh"). The term I/O is used to describe any program, operation or device that transfers data to or from a computer and to or from a peripheral device. Every transfer is an output from one device and an input into another. Devices such as keyboards and mice are input-only devices while devices such as printers are output-only. A writable CD-ROM is both an input and an output device.

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
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